light of the overall teachings of the disclosure. Accordingly, the particular arrangements disclosed are meant to be illustrative only and not limited to the scope of the present invention, which is to be given the full breadth of the following claims and all equivalents thereof.

What is claimed is:

1. A silicon carbide semiconductor device, comprising:

a first or second electrically conductive type substrate made of 4H silicon carbide and having a surface on one of a (000-1) c-plane and a (0001) Si-plane;

a drift layer formed on the substrate with the first electrically conductive type silicon carbide having a lower impurity concentration than that of the substrate;

a trench formed with a surface of the drift layer and having sidewalls formed with surfaces extending in one of a [11-20] direction and a [1-100] direction;

base regions, formed in the drift layer in areas on both sides of the trench such that the trench is sandwiched, which are made of the second electrically conductive type silicon carbide;

source regions, formed on upper layer portions of the base regions in contact with the sidewalls of the trench such that the trench is sandwiched, which are made of the first electrically conductive type silicon carbide having a higher concentration than that of the drift layer;

a gate oxide film, formed on an upper area of a bottom wall of the trench upon thermally oxidizing a surface of the trench, which has a thickness greater than that of each sidewall of the trench;

a gate electrode formed in the trench in an area above the gate oxide film;

first electrode electrically connected to the source regions, respectively;

a second electrode formed on the substrate at a rear surface thereof;

second electrically conductive type deep layers formed on the drift layer in areas spaced from the trench with the base regions being intervened each in a depth equal to or greater than a depth of the trench and having a concentration equal to or greater than that of the base regions; and

channel regions formed on surface areas of the base regions to allow an electric current to flow between the first and second electrodes via the source regions and the drift layer.

2. The silicon carbide semiconductor device according to claim **1**, wherein:

the silicon carbide semiconductor device takes the form of an inversion-type trench gate structure MOSFET;

wherein the base regions are held in contact with the sidewalls of the trench; and

wherein the channel regions are formed on the surface areas of the base regions upon controlling a voltage applied to the gate electrode.

3. The silicon carbide semiconductor device according to claim **1**, wherein:

the silicon carbide semiconductor device takes the form of an accumulation-type trench gate structure MOSFET; and

wherein the channel regions include first electrically conductive type channel layers, formed on surfaces of the trench in contact with the sidewalls of the trench so as to straddle the drift layer and the source regions, which are made of silicon carbide.

4. The silicon carbide semiconductor device according to claim **3**, further comprising:

second electrically conductive type contact regions, spaced in placement from the trench so as to sandwich the source regions to allow the base regions to be electrically connected to the first electrode, each of which has a higher concentration than that of each of the base regions; and

wherein the deep layers are placed beneath the contact regions to be unitarily formed with the contact regions, respectively.

5. The silicon carbide semiconductor device according to claim **4**, wherein:

each of the deep layers has a second electrically conductive type impurity concentration ranging from $1.0\times10^{17}/cm^3$ to $1.0\times10^{20}/cm^3$.

6. The silicon carbide semiconductor device according to claim **4**, wherein:

each of the deep layers has a depth ranging from 1.5 to 3.5 μm starting from a surface of each of the base regions.

7. The silicon carbide semiconductor device according to claim **1**, further comprising:

second electrically conductive type reserve layers, formed on the drift layer in areas below the trench and the deep layers, respectively, each of which has a lower concentration than that of each of the deep layers.

8. The silicon carbide semiconductor device according to claim **1**, further comprising:

low resistance regions, formed on the drift layer in areas each between the sidewall of the trench and the deep layer, each of which has a higher concentration than that of the drift layer.

9. The silicon carbide semiconductor device according to claim **7**, further comprising:

low resistance regions, formed in areas each between the sidewall of the trench, the deep layer and the reserve layer, each of which has a higher concentration than that of the drift layer.

10. The silicon carbide semiconductor device according to claim **1**, wherein:

the silicon carbide semiconductor device takes the form of an inversion-type trench gate structure MOSFET in which the channel regions are formed on the surface areas of the base regions upon controlling a voltage applied to the gate electrode;

the base regions are held in contact with the sidewalls of the trench; and

the deep layers include metallic layers spaced from the trench with the base regions being intervened and each formed in a depth equal to or greater than a depth of the trench whereby each of the metallic layers and the drift layer are operative to act as a Schockley diode.

11. The silicon carbide semiconductor device according to claim **1**, wherein:

the silicon carbide semiconductor device takes the form of an accumulation-type trench gate structure MOSFET in which the channel regions include first electrically conductive type channel layers, formed on surfaces of the trench in contact with the sidewalls of the trench so as to straddle the drift layer and the source regions and made of silicon carbide, whose channels are controlled upon controlling a voltage applied to the gate electrode; and

the deep layers include metallic layers spaced from the trench with the base regions being intervened and